10-23-00 A

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	BGA02US
First Inventor or Application Identifier	KIA SILVERBROOK
Title	METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT CARRIER
Express Mail Label No.	EK333430482US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 11] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 11]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3 73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [ ] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [X] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [X] Other: *Assembly and Packaging Section of the International Technology Road Map for Semiconductors, - 1999 Edition*

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment.*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

Prior application information *Examiner* _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* *24011* *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

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Name (Print/Type)	Kia Silverbrook	Registration No (Attorney/Agent)	
Signature		Date	October 18, 2000

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT ($) 395

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	*Kia Silverbrook*
Examiner Name	
Group Art Unit	
Attorney Docket No.	*BGA02US*

JC930 U.S. PRO 09/693484 10/20/00

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   Deposit Account Number
   Deposit Account Name
   ☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1 17
   ☐ Applicant claims small entity status See 37 CFR 1 27
2. [x] **Payment Enclosed:**
   [x] Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	(355)	Utility filing fee	355
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 355

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	11	-20** = 0	X	9	= 0
Independent Claims	1	- 3** = 0	X	40	= 0
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	(9)	Claims in excess of 20
102	80	202	(40)	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater, For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	(40)	Recording each patent assignment per property (times number of properties)	40
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1 129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	*Kia Silverbrook*	Registration No (Attorney/Agent)		Telephone	*+61-2-9818-6633*
Signature				Date	*October 18, 2000*

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Title of the Invention

METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT CARRIER

Field of the Invention

This invention relates to integrated circuit packages. More particularly, the invention relates to a method of manufacturing an integrated circuit carrier for an integrated circuit package.

Background to the Invention

Due to the ever-increasing number of connections (pincount) of integrated circuits, the use of ball grid array packages to connect integrated circuits to printed circuit boards is increasing. This facilitates the redistribution of a very fine pitch of flip-chip bump array of the integrated circuit to a much larger pitch ball grid array for attachment to the printed circuit board (PCB).

The carrier is often referred to as an interposer and can be fabricated from different materials such as ceramic, or a plastics material such as bismaleimide triazine (BT).

The carrier also functions as a heat sink by removing thermal energy from the integrated circuit by thermal conduction. Accordingly, the carrier is subjected to thermal strains.

In addition, an electronic package assembly comprising the integrated circuit, the carrier and the PCB has a number of different materials with different mechanical properties. Complex thermal stresses can occur inside the package during operation due to non-uniform temperature distributions, geometry, material construction and thermal expansion mismatches.

Typically, these days the integrated circuit is electrically connected to the carrier by a ball grid array of gold or solder bumps. Similarly, the carrier is electrically connected to the PCB by a further, larger ball grid array of solder balls. The thermo-mechanical stresses are typically severest at the solder ball interfaces between the PCB and the carrier. This can result in shearing of the solder ball connection. The problem is amplified by an increase in edge length of the carrier because of an increase in the thermal strain differences between the PCB and the carrier. An increase in edge length of the carrier is typically associated with an increase in the number of integrated circuit connections and solder balls.

Current ball grid array design is, presently, at the limit of reliability for typical integrated circuit pin counts.

Typically, a solder ball has a peak elastic shear strain value of around 0.08%. Computational experiments done by the applicant using a 500 micron thick solid Silicon carrier, 500 micron diameter solder balls at 1 millimeter pitch, a 700 micron thick PCB and a 16 millimeter side silicon chip indicated a peak shear strain value of 1.476% in the outermost ball of the package which is far above the plastic yield value of the solder ball.

This result is to be expected as the balls at the outermost edge of the package experience the greatest amount of translational shear.

As indicated in the publication of the Assembly and Packaging Section of the International Technology Road Map for Semiconductors, - 1999 Edition (copy attached), the most recent edition available at the time of filing the present application, in Table 59a at page 217, a pin count of a high performance integrated circuit has of the order of 1800 pins. The technology requirements in the near term, i.e. until the year 2005 indicate that, for high performance integrated circuits, a pin count exceeding 3,000 will be required for which, as the table indicates, there is, to date, no known solution. Similarly, in Table 59b of that publication, at page 219, in the longer term, until approximately the year 2014, a pin count for high performance integrated circuit packages of the order of 9,000 will be required. Again, as indicated in the table, there is no known solution for this type of package.

These aspects are the focus of the present invention.

Summary of the Invention

According to the invention there is provided a method of manufacturing an integrated circuit carrier the method including the steps of

providing a substrate;

demarcating at least one receiving zone for an integrated circuit on the substrate and a plurality of island-defining portions arranged about said at least one receiving zone; and

creating rigidity-reducing arrangements between neighboring island-defining portions by removing material from the substrate.

The method may include forming electrical contacts in said at least one receiving zone and forming an electrical terminal in each island-defining portion, each electrical terminal being electrically connected via a track of a circuitry layer to one of the electrical contacts.

Accordingly, the method may include forming the circuitry layer on a surface of the substrate by depositing a metal layer on the substrate. Then, the method may include etching the metal layer to form tracks.

The method may include demarcating said at least one receiving zone and the island-defining portions by means of a mask applied to a surface of the substrate.

The method may then include removing the material of the substrate to create the rigidity-reducing arrangements by etching through the substrate after the exposure of the substrate, carrying the mask, to light.

Preferably, the method includes forming the rigidity-reducing arrangements by means of a re-entrant etch to improve heat sink capabilities of the carrier.

The method may include creating secondary rigidity-reducing arrangements between each of those island-defining portions bordering said at least one receiving zone and said at least one receiving zone. Once again, the method may include creating the secondary rigidity-reducing arrangements by etching through the substrate.

The method may include forming the substrate from a wafer from undoped silicon having an insulating layer. The insulating layer may be used as a hard mask for the etch.

The method may include demarcating said at least one receiving zone by forming a recess in the substrate. The recess may be demarcated by etching the substrate.

Instead, the method may include demarcating said at least one receiving zone by forming a passage through the substrate, a region of the substrate surrounding the passage carrying the electrical contacts. Once again, the passage may be formed by etching the substrate.

Brief Description of the Drawings

The invention is now described by way of example with reference to the accompanying diagrammatic drawings in which:-

Figure 1 shows a schematic, plan view of part of a conceptual integrated circuit carrier;

Figure 2 shows a plan view of a part of an integrated circuit carrier, in accordance with the invention;

Figure 3 shows a perspective, sectional view of part of one embodiment of the integrated circuit carrier;

Figure 4 shows a perspective, sectional view of part of a second embodiment of the integrated circuit carrier;

Figure 5 shows a perspective, sectional view of part of a third embodiment of the integrated circuit carrier;

Figure 6 shows a perspective, sectional view of part of a fourth embodiment of the integrated circuit carrier;

Figure 7 shows a sectional, side view of one embodiment of the integrated circuit carrier, in use;

Figure 8 shows a sectional, side view of another embodiment of the integrated circuit carrier, in use;

Figure 9 shows, on an enlarged scale, the circled part 'A', of Figure 8;

Figure 10 shows, on an even greater enlarged scale, a sectional side view of part of the integrated circuit carrier;

Figure 11 shows a side view of yet a further embodiment of the integrated circuit carrier;

Figure 12 shows a sectional side view of still a further embodiment of the integrated circuit carrier;

Figure 13 shows a multi-chip module based on the integrated circuit carrier; and

Figure 14 shows a sectional side view of the multi-chip module based on the integrated circuit carrier.

Detailed Description of the Drawings

Referring to the drawings, an integrated circuit carrier, in accordance with the invention, is designated generally by the reference numeral 10. An integrated circuit carrier is shown in greater detail in Figure 2 of the drawings.

The integrated circuit carrier 10 has a receiving zone 12 for receiving an integrated circuit or chip 14 (Figure 7).

A plurality of island defining portions or islands 16 surround the receiving zone 12. Each island 16 has an electrical terminal 18 thereon to which a solder ball 20 is attach or reflowed.

Each island 16 is connected to its neighboring island or islands 16 via a rigidity reducing arrangement in the form of a serpentine member 22. This is shown in greater detail conceptually in Figure 1 of the drawings. As illustrated in Figure 1, each serpentine member 22 serves a spring-like function so that each island 16 has a degree of freedom of movement relative to its neighboring islands 16. Accordingly, the difference in expansion between a printed circuit board 24 (Figures 7 to 9) and the carrier 10 is compensated for by extension or retraction of the relevant serpentine members 22. As a result, the shear strain imparted to the solder balls 20 on the island

16 is considerably reduced and fatigue failure of the solder balls 20 is, correspondingly, reduced.

Various embodiments of the carrier 10 are now described with reference to Figures 3 to 6 of the drawings. In Figure 3 of the drawings, the carrier 10 has each island 16 connected to its neighboring island 16 by a serpentine member 22 which has a single, curved arm 26.

In the embodiment of the invention shown in Figure 4 of the drawings, each serpentine member 22 connects one island 16 to its neighboring island 16 by a pair of parallel arms 28 interconnected by an orthogonal bridging portion 30.

Each serpentine member 22 of the embodiment illustrated in Figure 5 of the drawings connects one island 16 to its neighboring island 16 via an arrangement having three arms 34 extending parallel to each other. Adjacent arms 34 are connected together by an orthogonal bridging portion 32.

In the embodiment illustrated in Figure 6 of the drawings, each serpentine member 22 which connects one island 16 to its neighboring island 16 has five parallel arms 36 with adjacent arms 36 being connected by an orthogonal bridging portion 38.

For ease of explanation, the embodiments illustrated in Figures 3 to 6 of the drawings shall be referred to below as the one arm 26 serpentine member 22, the two arm 28 serpentine member 22, the three arm 34 serpentine member 22, and the five arm 36 serpentine member 22, respectively.

As illustrated more clearly in Figures 7 to 9 of the drawings, those islands 16 surrounding the receiving zone 12 are connected to the receiving zone by a second rigidity reducing arrangement in the form of a zigzag element 40 which further aids in reducing the strain imparted to the solder balls 20.

Also, as illustrated in Figures 7 to 9 of the drawings, the integrated circuit 14 is electrically connected to electrical contacts 42 (Figure 2) in the receiving zone 12 via solder bumps 44.

The carrier 10 is formed from the same material as the integrated circuit 14. Accordingly, the carrier 10 is formed of silicon having an insulating layer of silicon dioxide. The insulating layer also serves as a hard mask for etching the serpentine members 22, as will be discussed in greater detail below.

In the manufacture of the integrated circuit carrier 10, a wafer 46 of silicon is provided. The wafer 46 can be single crystal silicon or polycrystalline silicon.

It is to be noted that the version of the carrier 10 shown in Figure 10 of the drawings is where the receiving zone 12 is on the same side of the carrier 10 as the pads 18 as shown in Figure 7 of the drawings. Where the receiving zone 12 is on an

opposite surface of the carrier 10, as shown in Figure 8 of the drawings, the circuitry layer is applied to both sides of the wafer 46. This is shown on a smaller scale in Figure 9 of the drawings. In this embodiment, each track 52 is electrically connected to its associated pad 18 via a plated through hole 58 extending through the wafer 46.

Referring now to Figures 11 and 12 of the drawings, two further embodiments of the carrier 10 are illustrated. With reference to the previous drawings, like reference numerals refer to like parts, unless otherwise specified.

In the examples illustrated, the receiving zone 12 is, instead of being demarcated on a surface of the carrier 10, a passage 60 defined through the carrier 10. The integrated circuit 14 is attached to a mounting means or retaining means in the form of a metallic lid 62 which is bonded to one surface of the carrier 10. An opposed surface of the integrated circuit 14 has bond pads for electrically connecting the integrated circuit to the carrier 10. It will be appreciated that, in this embodiment, the electrical contacts are arranged on that part of the carrier 10 surrounding the passage 60. In the embodiment illustrated in Figure 11 of the drawings, the interconnects are wire bonds 64. Either ball or wedge bonds can be used. In the embodiment illustrated in Figure 12 of the drawings, the interconnects are tape automated bond (TAB) films 66 or other planar connections such as beam leads.

Referring now to Figure 13 of the drawings, a development of the integrated circuit carrier is illustrated and is designated generally by the reference numeral 70. With reference to the previous drawings, like reference numerals refer to like parts, unless otherwise specified.

In this embodiment of the invention, the carrier 70 is a multi-chip module substrate 70 carrying a plurality of integrated circuits or chips such as those illustrated at 72, 74 and 76 in Figure 13. The chips 72, 74 and 76 are either carried on the surface of the carrier 70 or, as described above with reference to Figures 10 and 11, the chips are recessed in the carrier 70 as illustrated in Figure 14 of the drawings.

As indicated above, the serpentine members 22 may have different configurations such as the one arm 26 configuration, the two arm 28 configuration, the three arm 34 configuration or the five arm 36 configuration. Other configurations such as 4 arm or 6 or more arm configurations are also possible using finite element analyses, a results matrix for different carrier implementations, having different forms of serpentine members 22 and different ball arrays was generated. The matrix, which is set out below, contains results for ball grid arrays having rows of one to twenty-four balls, carriers of solid silicon, solid Al_2O_3, solid BT, a one arm 26 serpentine member

22, a two arm 28 serpentine member 22, a three arm 34 serpentine member 22 and a five arm 36 serpentine member.

No. of Balls in Row	1	4	8	16	24	100
Solid Si Interposer			1.08%	1.48%	1.61%	1.01%
Solid Al_2O_3 Interposer			0.667%	0.953%	1.077%	0.72%
Solid BT Interposer			0.126%	0.149%	0.150%	0.097%
One arm serpentine member			0.103%	0.0903%	0.085%	
Two arm serpentine member	0.47%	0.15%	0.147%	0.136%	0.128%	0.088%
Three arm serpentine member	0.22%	0.082%	0.079%	0.058%	0.056%	
Five arm serpentine member			0.025%	0.025%	0.013%	

As indicated above, the elastic strain limit for solder is around 0.08%. A row of solder balls is defined as from an edge of the receiving zone 12 to the edge of the carrier 10.

The results show that the peak solder ball strain value for solid carriers increases with an increasing number of solder balls 20 up to a certain point, due to the cumulative effect of thermo-mechanical strain between the PCB 24 and carrier 10. The solder ball strain actually goes down for the hundred ball implementation, probably due to a change in deflection shape of the solid silicon carrier. Peak strain still occurs in the outermost ball however although it is decreased because differential expansion between the carrier and the PCB is minimised. Also, the peak strain value of the solid carriers, apart from the BT carrier, is still, far in excess of the elastic strain limit for solder.

The serpentine member 22 implementations show a decrease in peak solder ball strain with increasing number of solder balls. This is due to the fact that the thermal strain mismatch is distributed over a greater number of solder balls 20 resulting in a deflected shape with less severe gradients. Smaller ball grid arrays, i.e. having fewer balls in a row, exhibit more severe deflection gradients that induce a concentrated load on either the innermost or the outermost solder ball 20.

Accordingly, it is a particular advantage of the invention that, due to the reduction of the peak strain with an increasing number of solder balls 20 there is no thermo-mechanical limit to the amount of integrated circuit pin connections. A line of 100 balls on all sides of the receiving zone 12 equates to a ball grid array of more than 40,000 balls, well in excess of expected requirements of 9,000 balls by 2014. Finite element calculations indicate that the peak solder ball strain is less than the elastic limit

of solder for carriers with three or more arm serpentine members, with 8 or more rows of balls. As the receiving zone is silicon, and therefore has the same coefficient of thermal expansion as a silicon integrated circuit, the strain on the bump connections from the integrated circuit 14 to the carrier 10 is minimised. This indicates that a silicon BGA with etched compliant regions as described herein can provide a definite solution to problems of failure from thermal cycling that currently limit the number of connections that can be made between a chip and a PCB using ball grid arrays. Also, as described above, with the provision of the serpentine members 22, a greater surface area is provided which is further enhanced by the re-entrant etch 50 such that the heat sink capability of the carrier 10 is enhanced. This also aids in the increase in the number of solder balls 20 which can constitute the array.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

I CLAIM:

1. A method of manufacturing an integrated circuit carrier, the method including the steps of

providing a substrate;

demarcating at least one receiving zone for an integrated circuit on the substrate and a plurality of island-defining portions arranged about said at least one receiving zone; and

creating rigidity-reducing arrangements between neighboring island-defining portions by removing material from the substrate.

2. The method of claim 1 which includes forming electrical contacts in said at least one receiving zone and forming an electrical terminal in each island-defining portion, each electrical terminal being electrically connected via a track of a circuitry layer to one of the electrical contacts.

3. The method of claim 2 which includes forming the circuitry layer on a surface of the substrate by depositing a metal layer on the substrate.

4. The method of claim 1 which includes demarcating said at least one receiving zone and the island-defining portions by means of a mask applied to a surface of the substrate.

5. The method of claim 4 which includes removing the material of the substrate to create the rigidity-reducing arrangements by etching through the substrate after exposure of the substrate, carrying the mask, to light.

6. The method of claim 1 which includes creating the secondary rigidity-reducing arrangements by etching through the substrate.

7. The method of claim 1 which includes forming the substrate from a wafer of undoped silicon having an insulating layer.

8. The method of claim 1 which includes demarcating said at least one receiving zone by forming a recess in the substrate.

9. The method of claim 8 which includes forming the recess by etching the substrate.

10. The method of claim 2 which includes demarcating said at least one receiving zone by forming a passage through the substrate, a region of the substrate surrounding the passage carrying the electrical contacts.

11. The method of claim 10 which includes forming the passage by etching the substrate.

ABSTRACT OF THE DISCLOSURE

A method of manufacturing an integrated circuit carrier includes providing a substrate. At least one receiving zone for an integrated circuit is demarcated on the substrate. A plurality of island-defining portions is arranged about each of the receiving zones. Rigidity-reducing arrangements are created between neighboring island-defining portions by removing material from the substrate.

Figure 10

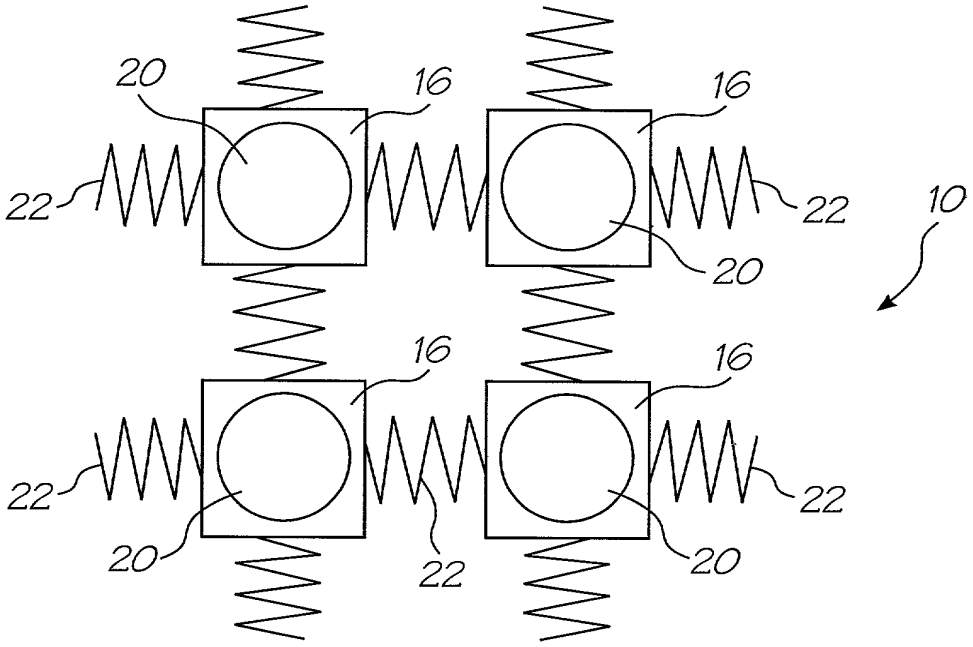

FIG. 1

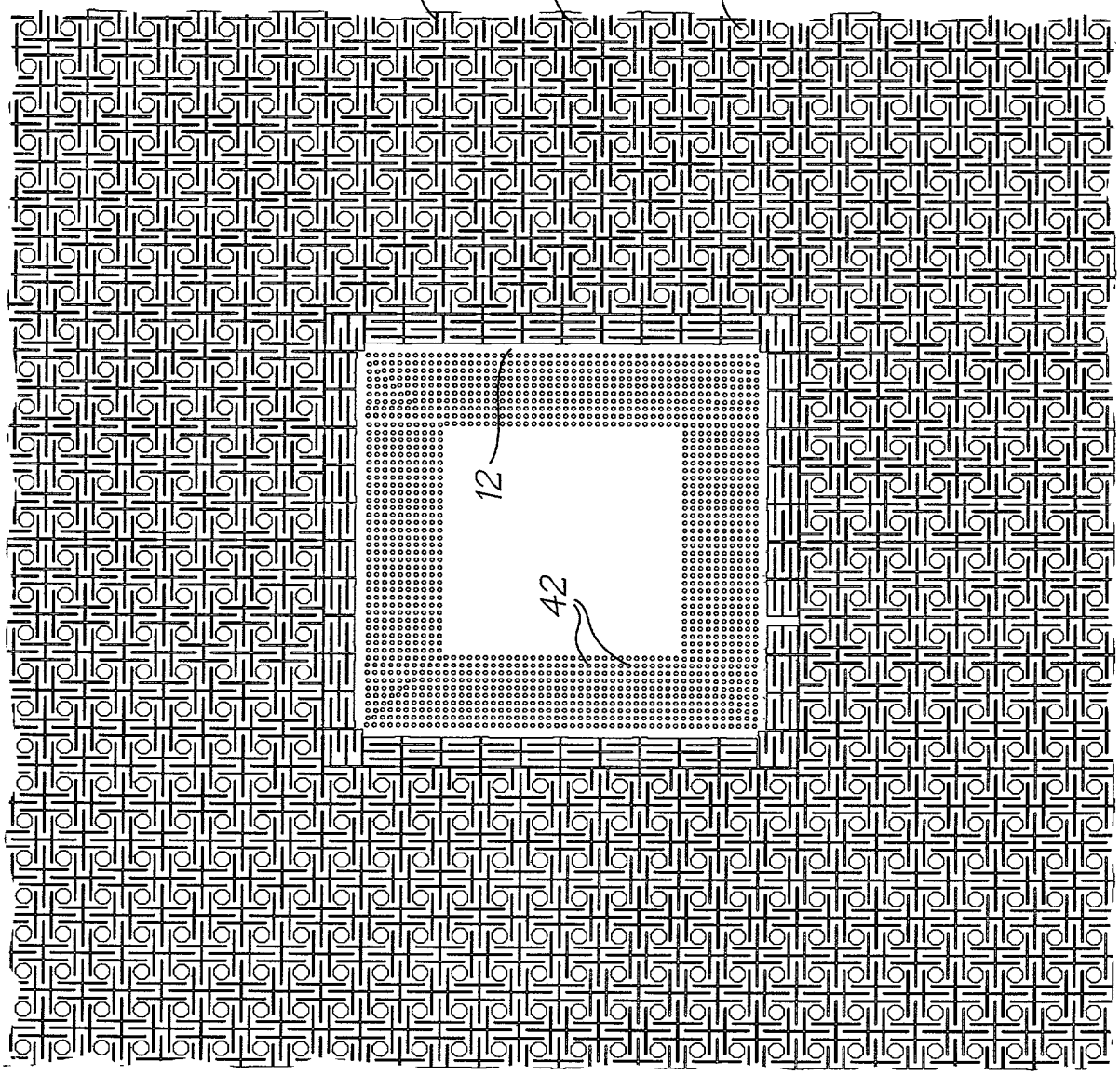

FIG. 2

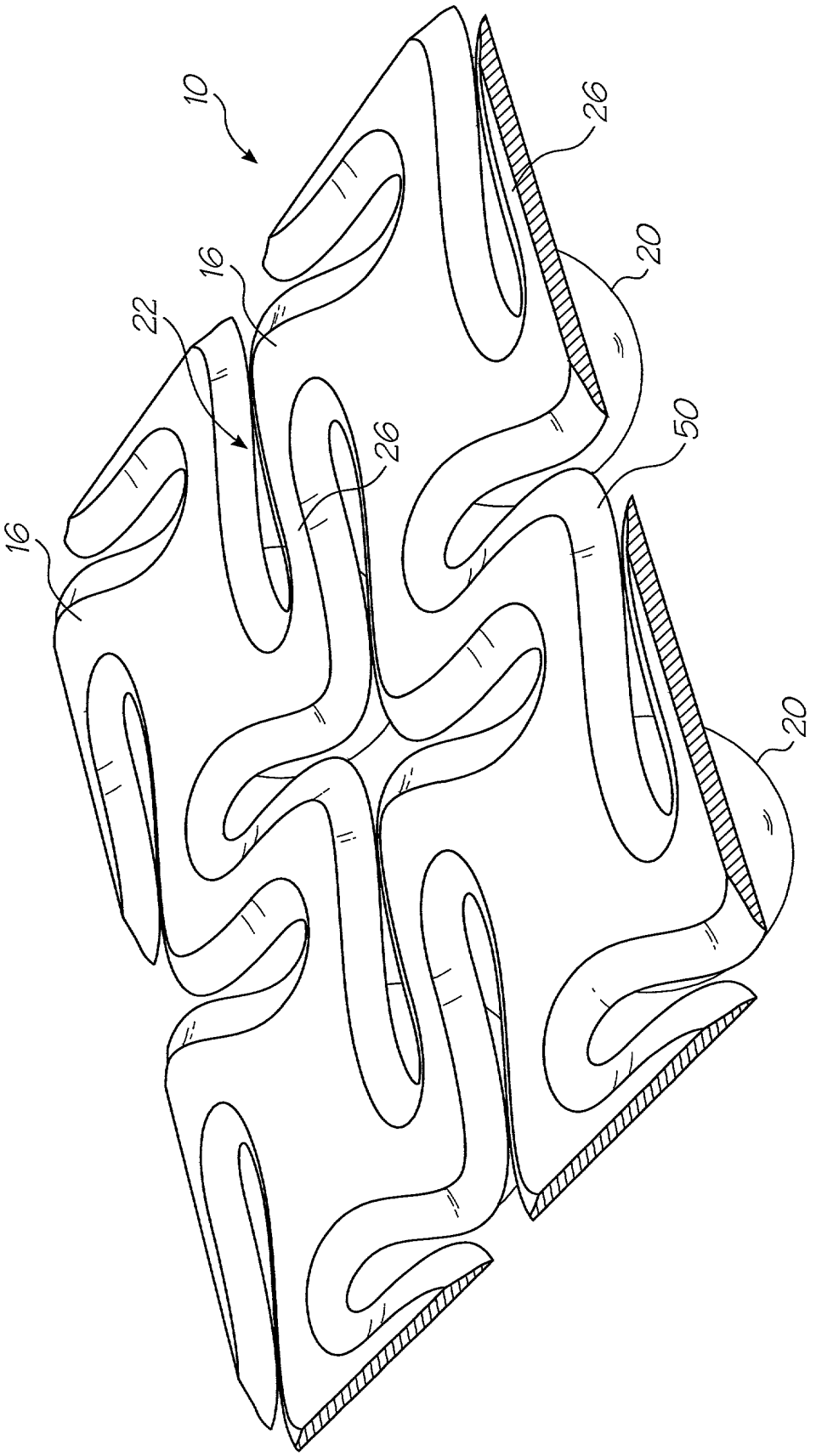

FIG. 3

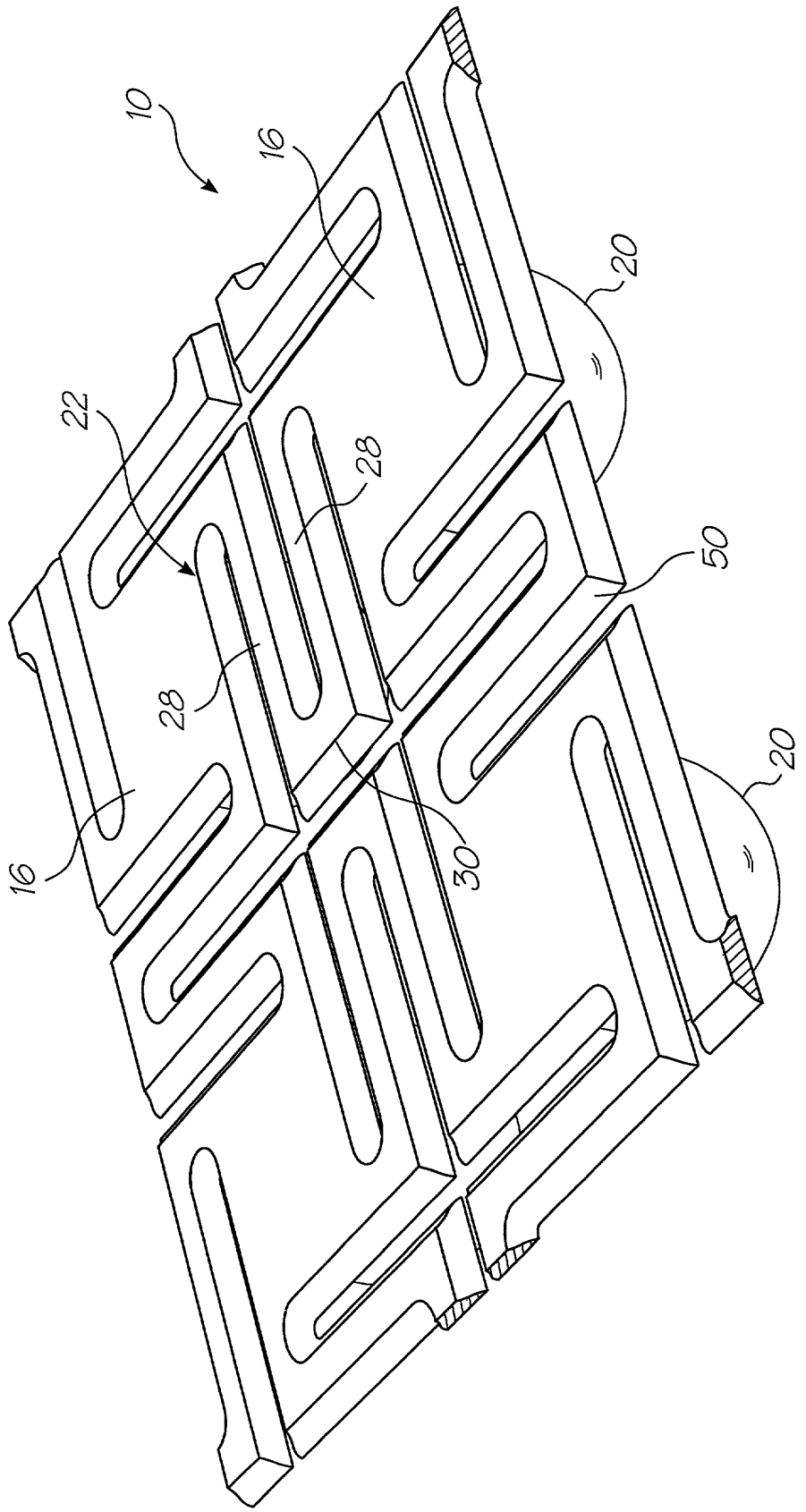

FIG. 4

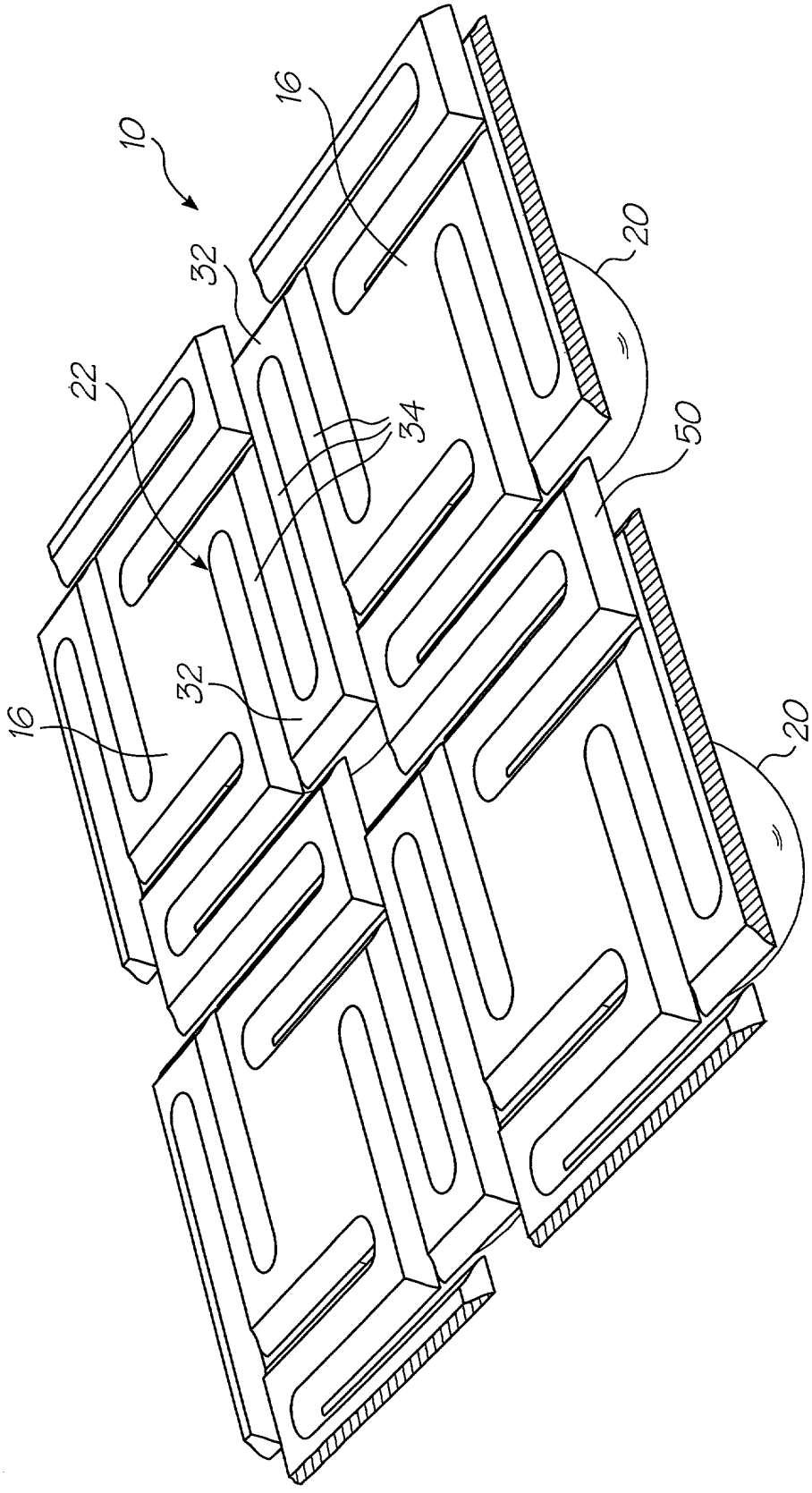

FIG. 5

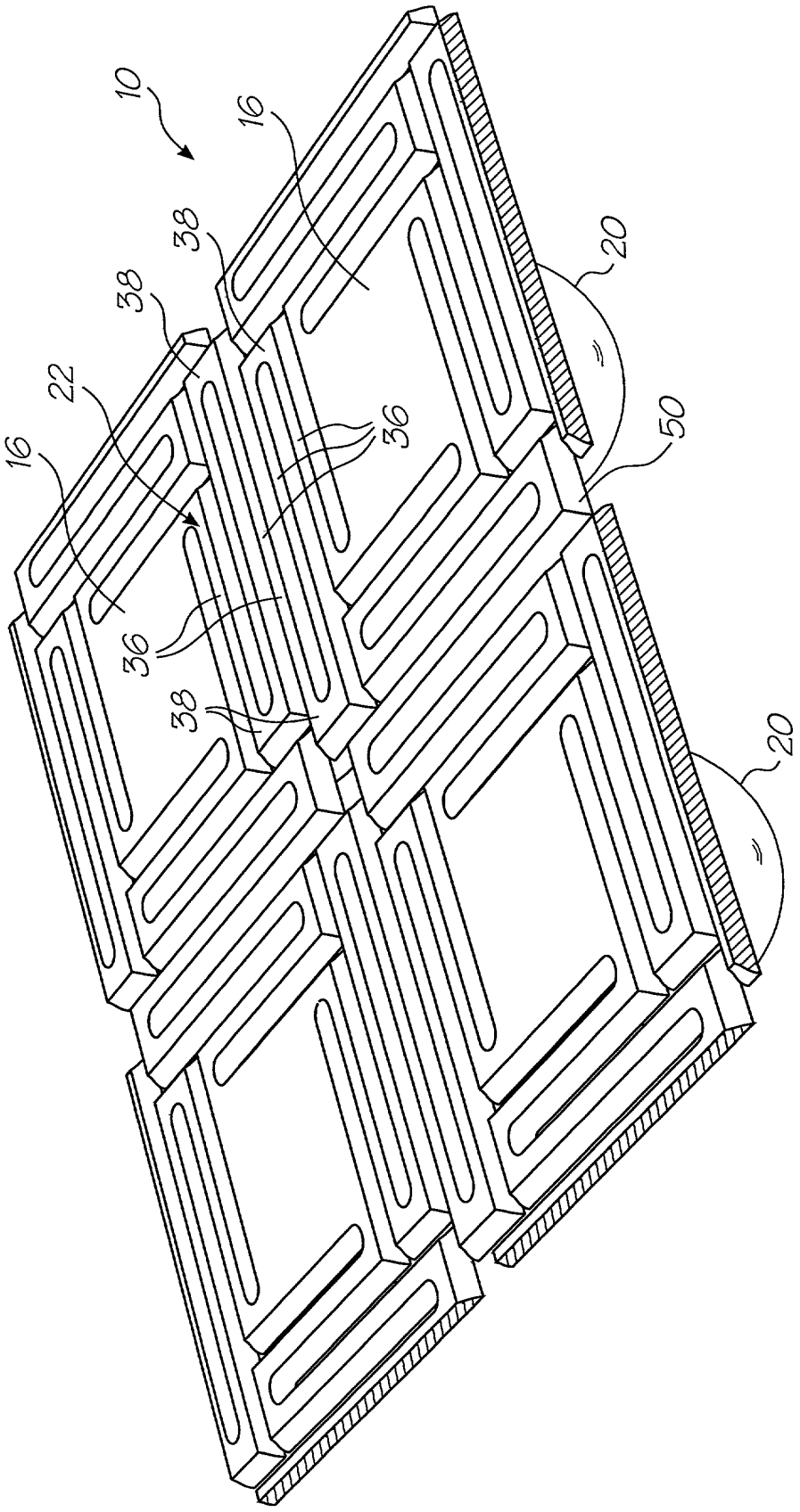

FIG. 6

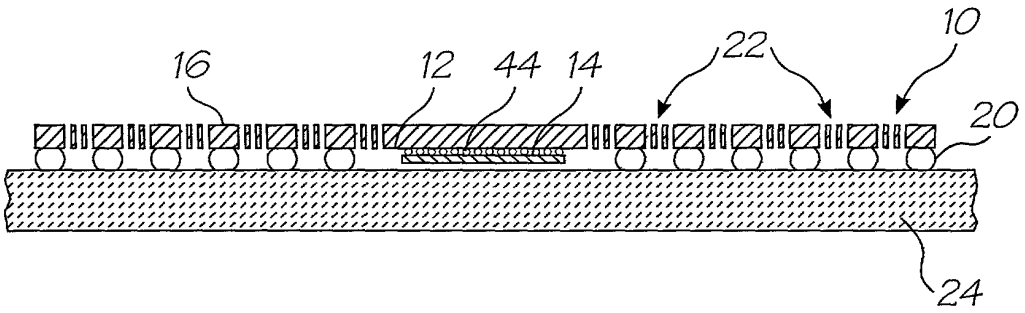

FIG. 7

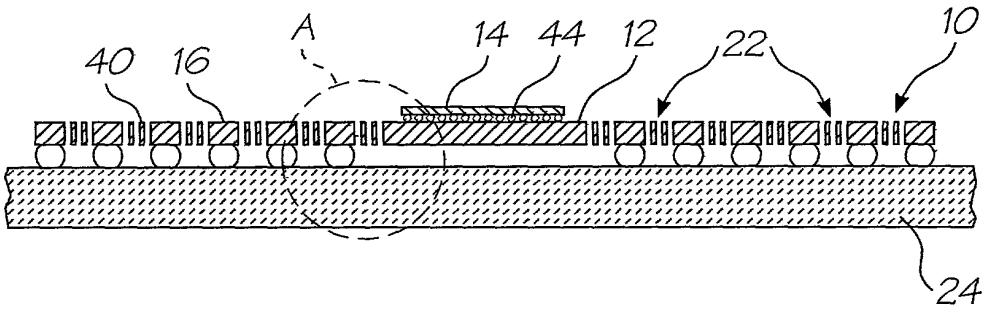

FIG. 8

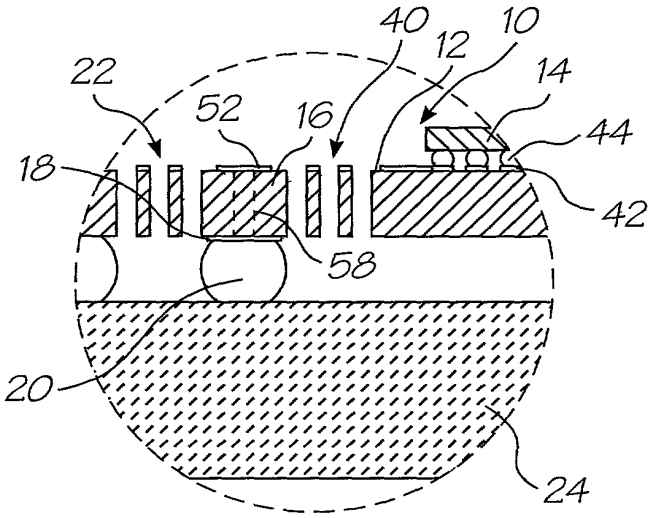

FIG. 9

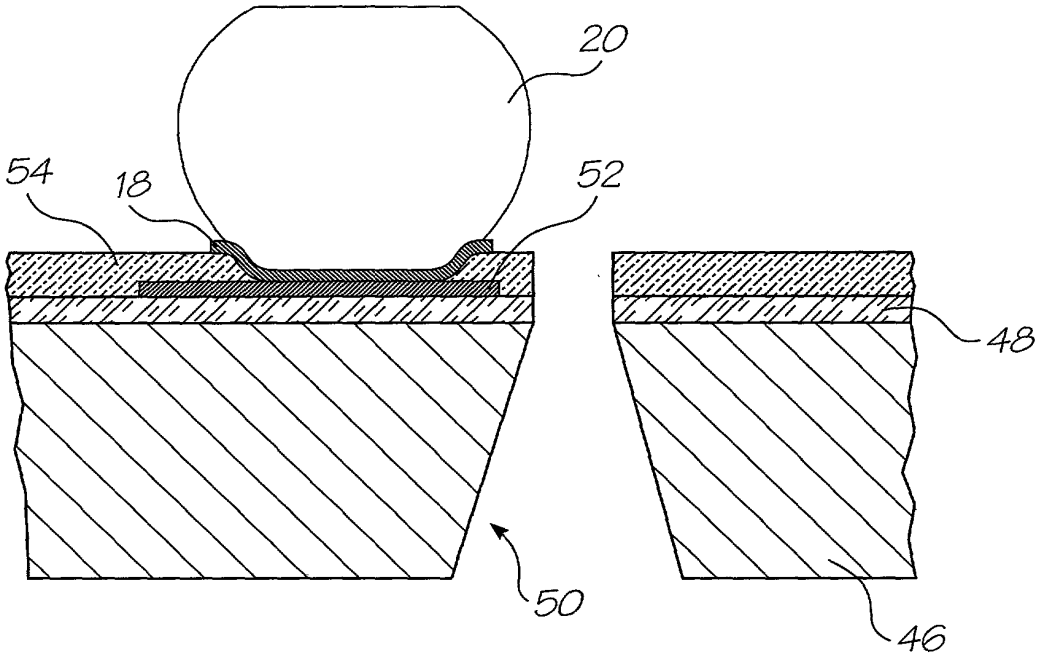

FIG. 10

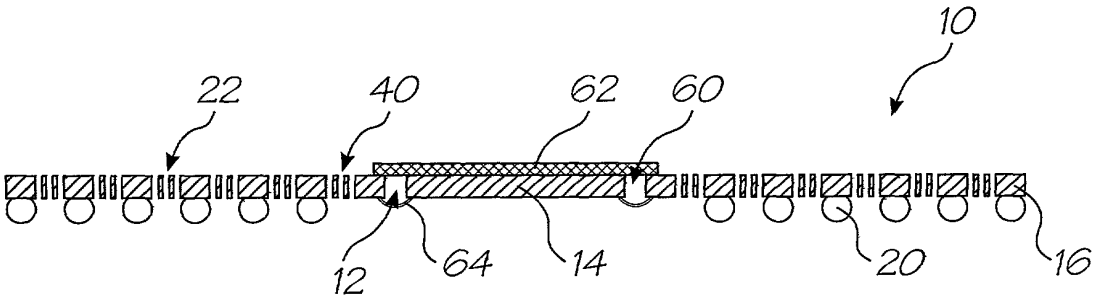

FIG. 11

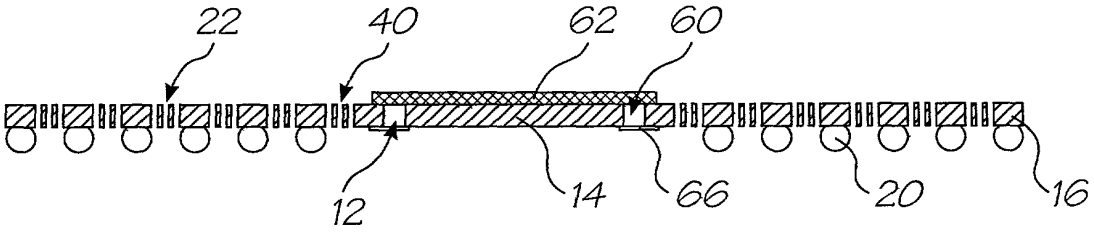

FIG. 12

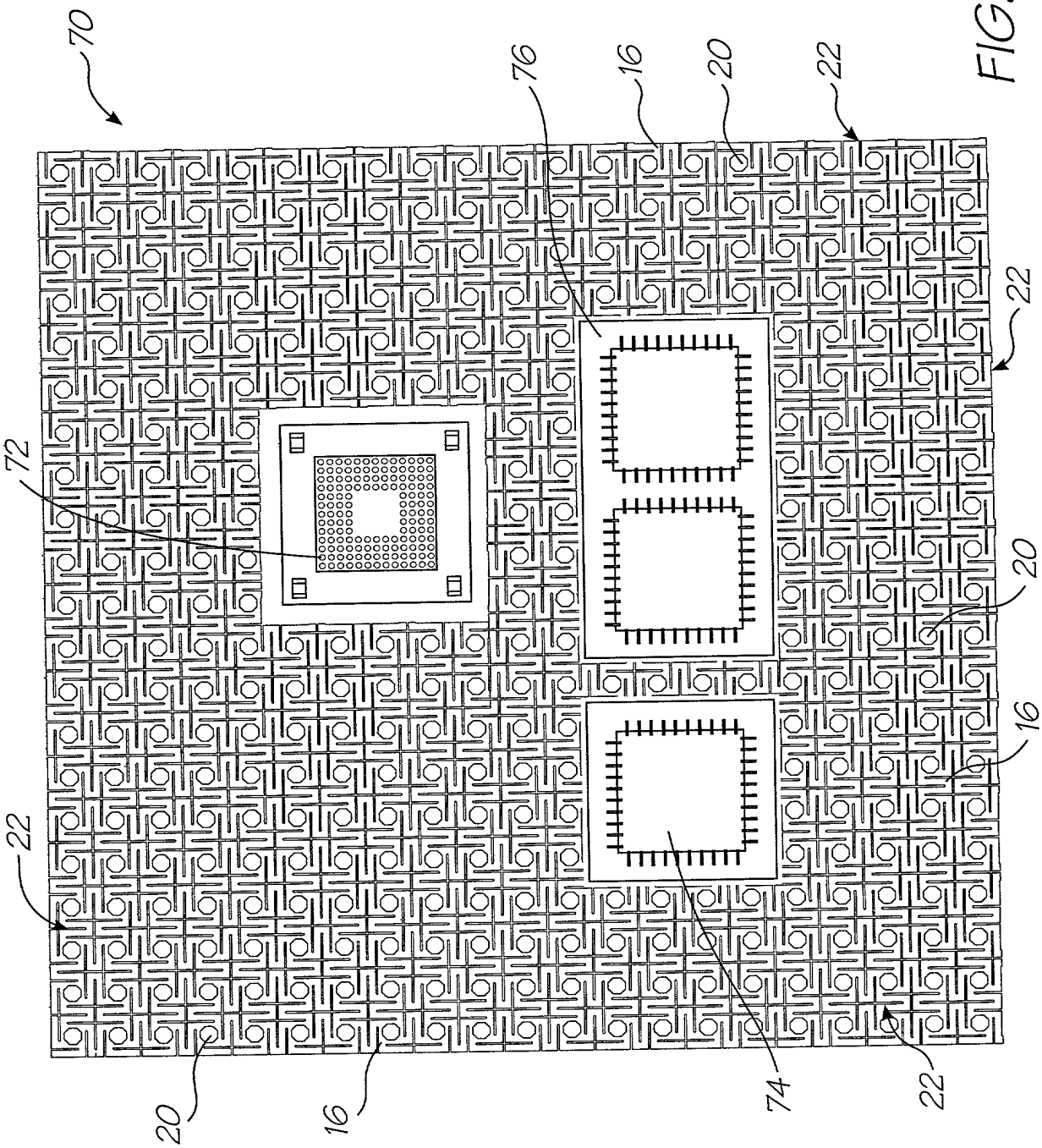

FIG. 13

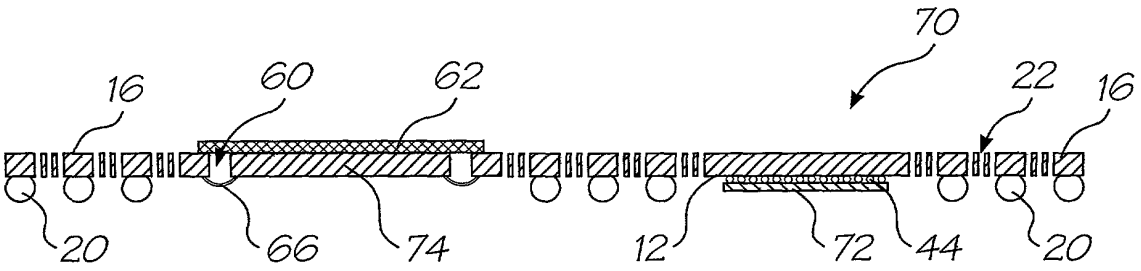

FIG. 14

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	*BGA02US*
First Named Inventor	*KIA SILVERBROOK*
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT CARRIER

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U S C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Burden Hour Statement. This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO. Assistant Commissioner for Patents, Washington, DC 20231.

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U S C 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: [x] Customer Number or Bar Code Label *24011* *OR* [x] Correspondence address below

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U S C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
KIA	*SILVERBROOK*

Inventor's Signature						Date	*Oct. 18, 2000*
Residence: City	*Balmain*	State	*NSW*	Country	*Australia*	Citizenship	*Austra-lian*
Post Office Address	*393 Darling Street*						
Post Office Address							
City	*Balmain*	State	*NSW*	ZIP	*2041*	Country	*Australia*

☐ Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto